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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/739,418	12/18/2003	Gregory E. Howard	TI-35903	1304

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EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/739,418	HOWARD, GREGORY E.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-15* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-9 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (U.S. Pat. 4803595) (previously applied) in view of Hayashi et al. (U.S. Pat. 6809268) (previously applied).

Kraus et al. disclose a semiconductor device comprising:

a) a plurality of spaced-apart substrate segments 1;

b) an integrated circuit chip 4 mounted on one of said segments; and

c) an interconnection layer 3 supporting said substrate segments (cover fig., column 2, lines 45-50).

Kraus et al. do not disclose the interconnection layer is a flexible interconnection layer.

However, Hayashi et al. disclose a semiconductor device comprising: a core substrate 2 composite material includes polymer resin having flexibility (cover fig., column 15, lines 20-28). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the semiconductor package of Kraus et al. by having the flexible interconnection layer because as taught by Hayashi et al., such flexible interconnection layer would provide the known purpose of assuring in

quality and reliability for the semiconductor device and less complex to implement the device.

- Regarding claim 2, Kraus et al. disclose that the device further includes a plurality of conductive vias 8 extending through one of said substrate segments connected to the terminals 5 or 7 of said chip; said vias also electrically and mechanically connected to pads and/or traces 13 on a first surface of said interconnection layer (cover fig.).
- Regarding claim 3, Kraus et al. disclose that the substrate segment 1 having the integrated circuit chip 4 mounted thereon is surrounded by a plurality of substrate segments on said interconnection layer, each substrate segment positioned over a plurality of external contacts 7 on the opposite surface of said interconnection layer.
- Regarding claims 5-6, Hayashi et al. disclose a semiconductor device having a substrate segment comprises a BT resin with a thickness of approximately 0.8mm (cover fig., column 6, lines 27-29). The substrate is made of bismaleimide triazine (BT) resin would have a tensile modulus of greater than 50 GPa.
- Regarding claim 7, Kraus et al. disclose that the integrated circuit chip contacts comprise flip chip bumps 7 (cover fig.).
- Regarding claim 8, Kraus et al. disclose that external contacts comprise solder balls [the plurality of balls on a surface of layer 3] (cover fig.).

- Regarding claim 9, Kraus et al. disclose that the connections [the plurality of balls on a surface of layer 3] between said substrate segments 1 and said interconnection layer 3 are comprised of solder (cover fig.).
- Regarding claim 12, Kraus et al. disclose a multi-chip module comprising:

a) a plurality of substrate segments 1 mounted on one surface of a interconnection layer 3;

b) a plurality of electronic components including integrated circuit chips and/or capacitors 2 and 4 mounted on the opposite surface of said interconnection layer;

c) said interconnection layer including means for connecting said substrate segments, and

d) a plurality of external contacts on said substrate segments [plurality of balls on the surface of interconnection layer 3] (cover fig., column 2, lines 45 et seq.).

Kraus et al. do not disclose the interconnection layer is a flexible interconnection layer.

However, Hayashi et al. disclose a semiconductor device comprising: a core substrate 2 composite material includes polymer resin having flexibility (cover fig., column 15, lines 20-28). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the semiconductor package of Kraus et al. by having the flexible interconnection layer because as taught by Hayashi et al., such flexible interconnection layer would provide the known purpose of assuring in quality and reliability for the semiconductor device and less complex to implement the device.

- Regarding claim 13, Kraus et al. disclose that the electronic components are interconnected to each other and to said external contacts by a plurality of conductive vias 8 extending through said substrate segments, and conductors 13 on and in said flexible interconnection layer.
- Regarding claim 14, Kraus et al. disclose that the substrate segments are positioned atop a plurality of external solder ball contacts on the second surface of said interconnection layer (cover fig.).

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (U.S. Pat. 4803595) (previously applied) in view of Hayashi et al. (U.S. Pat. 6809268) (previously applied) and further in view of Tada et al. (U.S. Pat. 5647999) (previously applied).

Kraus et al. also disclose that the flexible interconnection layer 3 comprising one or more levels of conductive traces connecting selected layers.

Kraus et al. and Hayashi et al. do not explicitly disclose the flexible interconnection layer comprises a low dielectric polymeric film having a tensile modulus in the range of 2 to 10 Gpa.

However, Tada et al. disclose a semiconductor device comprising an interconnection layer has a low dielectric polymeric film having a tensile modulus in the range of 2 to 10 GPa (column 4, lines 48-52). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of the above combination by having the flexible interconnection layer comprises a low dielectric polymeric film having a tensile modulus in the range of 2 to

10 Gpa because as taught by Tada et al., such polymeric film having a tensile modulus in the range of 2 to 10 GPA would increase the rigidity of the polymeric member.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (U.S. Pat. 4803595) (previously applied) in view of Hayashi et al. (U.S. Pat. 6809268) (previously applied) and further in view of Arima et al. (U.S. Pat. 5375042) (previously applied).

Kraus et al. and Hayashi et al. substantially discloses all the limitations as claimed above except for a preformed cap covering the integrated circuit chip and its interconnections.

However, Arima et al. disclose a semiconductor device comprising: a preformed cap 9 covering the integrated circuit chip 6 and its interconnections 8 (cover fig., column 4, lines 49-51). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of the above combination by having a preformed cap covering the integrated circuit chip and its interconnections because as taught by Arima et al., such preformed cap would protect the integrated circuit chip and its interconnections (cover fig.).

5. Claims 12 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn et al. (U.S. Pat. 6586835) (previously applied) in view of Hayashi et al. (U.S. Pat. 6809268) (previously applied).

- Regarding claim 12, Ahn et al. disclose a multi-chip module comprising:

a) a plurality of substrate segments 125 mounted on one surface of a interconnection layer 110;

b) a plurality of electronic components including integrated circuit chips 125 mounted on the opposite surface of said interconnection layer;

c) said interconnection layer including means for connecting said substrate segments, and

d) a plurality of external contacts on said substrate segments 131 (fig. 1A, column 4, lines 55 et seq.).

Kraus et al. do not disclose the interconnection layer is a flexible interconnection layer.

However, Hayashi et al. disclose a semiconductor device comprising: a core substrate 2 composite material includes polymer resin having flexibility (cover fig., column 15, lines 20-28). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the semiconductor package of Ahn et al. by having the flexible interconnection layer because as taught by Hayashi et al., such flexible interconnection layer would provide the known purpose of assuring in quality and reliability for the semiconductor device and less complex to implement the device.

- Regarding claim 15, Ahn et al. disclose that the electronic components 125 are mechanically and electrically connected on the first surface of said interconnection layer and the second surface of said interconnection layer 110 is connected to a plurality of substrate segments 125.

Allowable Subject Matter

Claim 16 is objected (see the examiner's statement of reasons for the indication of allow subject matter in the previous office action).

Response to Arguments

Applicant's arguments filed 5/30/06 have been fully considered but they are not persuasive.

- The applicant argues that there is no motivation to combine the references of Kraus et al. in view of Hayashi et al.

The arguments have been fully considered but they are not persuasive because the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

- In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case:

Kraus et al. disclose a semiconductor device comprising:

a) a plurality of spaced-apart substrate segments 1;

b) an integrated circuit chip 4 mounted on one of said segments; and

c) an interconnection layer 3 supporting said substrate segments (cover fig., column 2, lines 45-50).

Kraus et al. or Ahn et al. substantially disclose all the limitations as claimed above except for the interconnection layer is a flexible interconnection layer.

However, Hayashi et al. disclose a semiconductor device comprising: a core substrate 2 composite material includes polymer resin having flexibility (cover fig., column 15, lines 20-28). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the semiconductor package of Kraus et al. by having the flexible interconnection layer because as taught by Hayashi et al., such flexible interconnection layer would provide the known purpose of assuring in quality and reliability for the semiconductor device and less complex to implement the device.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN

HOAI PHAM
PRIMARY EXAMINER